AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 3, line 17 with the following rewritten paragraph:

-- ~~By the way, in a patent document 1 (~~Japanese Patent Laid-Open Publication No. 188495/2003~~), there is disclosed an invention of~~(hereinafter "JP '495") discloses a process for producing a printed wiring board comprising subjecting a metal coated polyimide film, which has a first metal layer formed on a polyimide film by a dry film-forming method and a second metal layer having conductivity that is formed by plating on the first metal layer, to etching to form a pattern, wherein after the etching, the etched surface is subjected to cleaning treatment with an oxidizing agent. ~~In~~ Example 5 of ~~this patent document 1, an example comprising~~JP '495 discloses the steps of plasma depositing a nickel-chromium alloy in a thickness of 10 nm and then depositing copper in a thickness of 8 μm by plating ~~is shown~~. --

Please replace the paragraphs beginning at page 5, line 3 and ending at page 7, line 6 with the following rewritten paragraphs:

-- As described in ~~the above publication~~JP '495, a comb-shaped electrode is formed, and a wiring pattern for forming the comb-shaped electrode is subjected to plating. This plating is generally carried out as follows. The wiring pattern formed is coated with a solder resist ink in such a manner that the terminals (inner lead, outer lead) are exposed, then the solder resist ink is cured to form a solder resist layer, and the exposed terminals are plated. At the terminals formed through such steps as described in the above publication, however, it is difficult to effectively prevent occurrence of migration from the first metal layer formed on the polyimide film.

~~In paragraphs~~Paragraphs [0004] and [0005] of ~~a patent document 2 (~~Japanese Patent Laid-Open Publication No. 282651/2003~~), it is described that~~(hereinafter "JP '651") discloses a metal layer 1 made of an alloy of copper and that a metal other than copper is provided on a surface of a flexible insulating film 2 in order to ensure adhesion strength between the flexible insulating film and a wiring pattern, and then on a surface of the metal layer 1 a copper foil is arranged to form a composite, and from the composite a flexible wiring board is produced. ~~It is further described~~JP '651 further discloses that at the periphery

of the lower part of the lead of the wiring pattern formed by the use of such a composite, the metal layer 1 remains as the unremoved portion as shown in Fig. 5, and it is also described that because of the unremoved portion, abnormal deposit 6 of the plating metal is formed. Moreover, it is described that at the abnormal deposit 6 of the plating metal, a crystal of tin grows and becomes a "whisker", and because of the whisker, a short-circuit takes place in the wiring pattern. That is to say, if the metal layer 1 provided to ensure adhesion strength of the wiring pattern is left as it is and if a tin plating layer is formed on the surface of the metal layer 1, a whisker is produced from the thus formed tin plating layer. ~~In the document 2, therefore,~~Accordingly, in JP '651 the metal layer 1 is completely removed, as described in ~~a~~ paragraph [0023] thereof.

However, it is extremely difficult to completely remove the metal layer 1 from the outer periphery of the wiring pattern. In the process described in ~~the patent document 2~~ JP '651, the metal layer 1 remains as it is at the outer periphery of the lower part of the wiring pattern though the amount is trace, and production of whiskers from the tin plating layer attributable to the residual metal layer 1 cannot be completely prevented.

~~Patent document 1: Japanese Patent Laid-Open Publication No. 188495/2003~~

~~Patent document 2: Japanese Patent Laid-Open Publication No. 282651/2003~~

~~DISCLOSURE OF THE INVENTION~~ --

Please replace the paragraph beginning at page 8, line 5 with the following rewritten paragraph:

-- ~~MEANS TO SOLVE PROBLEM~~SUMMARY OF THE INVENTION --

Please DELETE the section heading at page 11, line 8.

Please replace the paragraphs beginning at page 12, line 13 and ending at page 13, line 10 with the following rewritten paragraphs:

~~Fig. 1 is~~Figs. 1(A) – (J) are a group of views showing sections of boards in an embodiment of the process for producing a printed wiring board of the present invention~~.~~;

~~Fig. 2 is~~Figs. 2(A) – (I) are a group of views showing sections of boards in another embodiment of the process for producing a printed wiring board of the present invention~~.~~;

Fig. 3 is a sectional view of an embodiment of the printed wiring board of the present invention~~.~~;

Fig. 4 is a sectional view of another embodiment of the printed wiring board of the present invention~~.~~;

Fig. 5 is a SEM photograph showing an edge of a wiring on an insulating film before microetching treatment~~.~~;

Fig. 6 is a SEM photograph showing an edge of a wiring on an insulating film after microetching treatment~~.~~; and

~~Fig. 7 is~~Figs. 7(A) – (C) are a group of schematic perspective views showing a wiring pattern before treatment with a first treating solution (Fig. 7(A)), a wiring pattern after treatment with a first treating solution (Fig. 7(B)) and a wiring pattern after microetching treatment (Fig. 7(C)).

Please replace the section heading beginning at page 13, line 22 with the following rewritten paragraph:

-- ~~BEST MODE FOR CARRYING OUT~~DETAILED DESCRIPTION OF THE INVENTION --

Please replace the paragraph beginning at page 15, line 8 with the following rewritten paragraph:

-- The insulating film 11 has an average thickness of usually 7 to 80 μm, preferably 7 to 50 μm, particularly preferably 15 to 40 μm. The printed wiring board of the invention is suitable as a thin board, so that it is preferable to use a thinner polyimide film. The surface of the insulating film 11 may have been subjected to surface roughening treatment using a hydrazine-KOH solution, plasma treatment or the like in order to enhance adhesion to the below-described base metal layer ~~13~~12. --

Please replace the paragraph beginning at page 16, line 22 with the following rewritten paragraph:

-- After the base metal layer 12 is formed as above, a conductive metal layer 20 is formed on the surface of the base metal layer 12, as shown in Fig. ~~2(D)~~(2C). The metal for forming the conductive metal layer 20 employable in the invention is, for example, copper or a copper alloy. The conductive metal layer 20 can be formed by a plating method. The plating method used herein is electroplating or electroless plating. --

Please replace the paragraphs beginning at page 19, line 9 and ending at page 20, line 22 with the following rewritten paragraphs:

-- After the conductive metal layer 20 is formed as above, the surface of the conductive metal layer 20 is coated with a photosensitive resin, and the photosensitive resin is exposed to light and developed to form a desired pattern 15 made of the photosensitive resin, as shown in Fig. 1(E) and Fig. ~~2(E)~~2(D). As the photosensitive resin, a photosensitive resin of such a type as is cured by irradiation with light may be used, or a photosensitive resin of such a type as is softened by irradiation with light may be used.

Then, using the pattern 15 formed from the photosensitive resin as a masking material, the conductive metal layer 20 is selectively etched to form a desired wiring pattern, as shown in Fig. 1(F) and Fig. ~~2(F)~~2(E).

The etching agent used herein is an agent for etching the conductive metal, and examples of such conductive metal etching agents include an etching solution containing ferric chloride as a major ingredient, an etching solution containing cupric chloride as a major ingredient, and an etching solution of sulfuric acid + hydrogen peroxide. The etching solution for the conductive metal can etch the conductive metal layer 20 with excellent selectivity to form a wiring pattern, and besides, it has a considerable etching function for the base metal present between the conductive metal layer 20 and the insulating film 11. Therefore, when etching is carried out using the above-mentioned conductive metal etching agent, the base metal layer 12 can be etched to such an extent that the base metal layer remains as an extremely thin layer of about several nm on the surface of the insulating film 11, as shown in Fig. 1(F) and Fig. ~~2(F)~~2(E). That is to say, between the wiring patterns, the base metal layer becomes an extremely thin layer, but below the wiring pattern formed from the conductive metal layer, the base metal layer is not etched and has the same thickness as the initial thickness. --

Please replace the paragraph beginning at page 22, line 11 with the following rewritten paragraph:

-- By the above treatment, such a protrusion 21a of the base metal remaining on the side surface of the wiring pattern and such a base metal layer 21b remaining between the wirings as shown in Fig. 7(A) are dissolved and removed, as shown in Fig. 7(B), and the shortest distance W between the base metal layers constituting the wiring patterns is widened (see Fig. 1(I), Fig. 1(J), Fig. ~~2(I)~~2(H), Fig. ~~2(J)~~2(I), Fig. 7, etc.). --

Please replace the paragraphs beginning at page 24, line 6 and ending at page 25, line 17 with the following rewritten paragraphs:

-- After the treatment with the first treating solution capable of dissolving Ni is carried out, the Cu pattern is selectively microetched by any one of a potassium persulfate ($K_2S_2O_8$) solution, a sodium persulfate ($Na_2S_2O_8$) solution and a solution of sulfuric acid + H_2O_2 to selectively slightly dissolve (retreat) the pattern composed of the conductive metal and thereby project the base metal layer (seed layer) from the conductive metal layer. However, if the contact time with the etching solution is long in this ~~microetheing~~microetching step, copper that is a conductive metal for forming the wiring pattern is dissolved in a large amount and the wiring pattern itself is thinned, so that the contact time of the wiring pattern with the etching solution in the ~~microetheing~~microetching step is in the range of usually 2 to 60 seconds, preferably 10 to 45 seconds.

After the conductive metal layer 20 is retreated as above in the ~~microetheing~~microetching step, the surface of the ~~insulting~~insulating film 11 where the wiring pattern has not been formed is finally treated with a second treating solution capable of dissolving Cr and the insulating film such as a polyimide film. That is to say, in the present invention, a treatment with a first treating solution capable of dissolving Ni is carried out, then microetching is carried out when needed, and then a treatment with a second treating solution capable of dissolving a part of Cr remaining as the base metal layer (seed layer) and capable of oxidizing/passivating the undissolved Cr is carried out, whereby most of the base metal layer 12 can be removed and Cr remaining in a thickness of several tens Å on the surface of the insulating film 11 can be oxidized and passivated. Accordingly, by the use of the second treating solution, the base metal layer 12 can be removed and the residual Cr can be oxidized and passivated, as shown in Fig. 1(I) and Fig. ~~2(I)~~2(H). --

Please replace the paragraph beginning at page 27, line 18 and continuing onto page 28 with the following rewritten paragraph:

-- After the wiring pattern is formed as above, concealing plating treatment is preferably carried out so as to conceal at least the base metal present as the side wall of the lower part of the wiring pattern. That is to say, in the printed wiring board of the invention, after formation of a wiring pattern and before formation of a solder resist layer, an exposed portion of the base metal layer 12 present at the bottom of the wiring pattern may be concealed with a concealing plating layer 16, as shown in Fig. 1(J), Fig. ~~2(J)~~(2I), Fig. 3 and Fig. 4. The concealing plating layer 16 has only to conceal at least the base metal layer 12 present at the bottom of the wiring pattern. The concealing plating layer 16, however, may be formed on the whole surface of the wiring pattern. The concealing plating layer thus formed is at least one layer selected from the group consisting of a tin plating layer, a gold plating layer, a nickel-gold plating layer, a solder plating layer, a lead-free solder plating layer, a Pd plating layer, a Ni plating layer, a Zn plating layer and a Cr plating layer. Of these, a tin plating layer, a gold plating layer, a Ni plating layer, a nickel-gold plating layer are particularly preferable in the present invention. It is also possible that the wiring pattern is partially coated with a solder resist prior to plating and the exposed portion is plated with the above-mentioned metal, as described later. --

Please DELETE the section heading on page 53, line 1.